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APPLICATION

FOR

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TITLE: FORMING STRAINED SOURCE DRAIN JUNCTION FIELD EFFECT TRANSISTORS

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FORMING STRAINED SOURCE DRAIN JUNCTION FIELD EFFECT TRANSISTORS

Background

This invention relates generally to integrated circuits and, particularly, to techniques for making metal oxide semiconductor field effect transistors (MOSFETs).

Progressively, integrated circuits are being made to smaller and smaller dimensions. Producing smaller dimensions generally means forming junctions for integrated circuit transistors that are shallower. These shallower junctions may have relatively low resistivity to maintain the current drive of the resulting transistors. Generally, producing lower resistance junctions involves increasing junction doping concentration. However, producing shallower junctions while increasing doping concentration may be difficult because of the limits imposed by dopant solid solubility in silicon.

In other words, it is desirable to make shallow, heavily doped junctions, but these two goals may be inconsistent with one another. In the past, junctions have been scaled using reduced energy ion implants and increased thermal ramp speeds in rapid thermal processing hardware. Increasing the ramp speed of the rapid thermal processing thermal anneal process allows a higher peak temperature that may improve solid solubility. The increase in solid

solubility allows the incorporation of more dopants and, hence, lower sheet resistance for the same junction depth. Similarly, the faster anneal times reduce the amount of dopant diffusion.

The ion implant energy of the source/drain implant and source/drain extensions also contributes to a shallower junction. An ion implant can produce shallow, very high concentrations of dopants, but conventional rapid thermal processing technology cannot activate anymore dopant. The concentration of the source/drain extensions has reached the solid solubility limit of conventional rapid thermal processing.

Thus, there is a need for still shallower junctions while maintaining adequate resistivity.

Brief Description of the Drawings

Figure 1 is an enlarged cross-sectional view of one embodiment of the present invention at an early stage of manufacture;

Figure 2 is an enlarged cross-section of the embodiment shown in Figure 1 after further processing in accordance with one embodiment of the present invention;

Figure 3 is an enlarged cross-sectional view of the embodiment shown in Figure 2 after further processing;

Figure 4 is an enlarged cross-sectional view of the embodiment shown in Figure 3 after further processing;

Figure 5 is an enlarged cross-sectional view of the embodiment as shown in Figure 4 after further processing; and

Figure 6 is a graph of concentration versus depth for embodiments of the present invention.

Detailed Description

Referring to Figure 1, initially a cap layer 12 may be deposited on a polysilicon gate structure 14 to block implant of germanium into the polysilicon. This prevents both the excessive sputtering of the polysilicon by the high dose germanium implant and limits the germanium content. This is desirable because high concentrations of germanium retards the boron diffusion which will negatively impact poly depletion in the gate.

The gate structure 14 may be defined over a semiconductor structure 10.

Removeable spacers 16 may be deposited and patterned to achieve the structure shown in Figure 2. Then, the spacers 16 may act as masks, together with the cap layer 12, for a germanium high dose implant as shown in Figure 3. By "high dose," it is intended to refer to a germanium implant that is of sufficiently high dose and energy to produce a substantial amount of strain in the resulting junction. For example, in some advantageous embodiments, the germanium implant dosage may be from about 2.0E16 to

6.0E16 atoms/cm2 at energies of at least 20 keV. In some embodiments an energy of about 50 keV is used.

In some embodiments, the germanium implant may also be deep enough to avoid consumption by a salicide. In some embodiments, this means that the implant is sufficient to produce an implanted depth greater than about 150 Angstroms.

Referring to Figure 4, the spacers 16 may be removed, leaving the exposed germanium implanted regions 17 in the substrate 10. At this point, the P-type source/drain extension implant may be done. In one embodiment, the P-type source/drain extension implant may be Boron 11. As a result of the Boron implant, an implanted region 18 may be formed that overlaps the implanted region 16 that includes germanium as shown in Figure 5.

Thereafter, conventional source/drain processing may be implemented, including the formation of a spacer for forming the deep source/drain regions of conventional source/drain junctions.

The addition of the high dose germanium implant to regions of high boron dose may produce favorable lattice interactions between boron and germanium. This may reduce defect, improve solid solubility and reduce boron diffusion, in some embodiments. Of course, the resulting junctions may be shallower and have lower resistivity.

The addition of the high dose germanium implants also adds strain of the right sign to improve hole mobility for PMOS devices. The strained germanium and boron doped junctions behave like a classical alloy. The strain is reduced with increasing boron concentration for constant germanium dose. Advantageously, the implants are deep enough to avoid complete consumption by salicide formation.

A strained germanium source/drain can be implanted with a deep/high dose implant after spacer deposition, but before the high dose boron source drain implant. As shown in Figure 2, a spacer 16 may be utilized in connection with the germanium implant. The spacer 16 may reduce gate edge damage in some cases as a result of implant straggle. After the removal of the spacer 16, in some embodiments, a poly reoxidation step may be done prior to doing a source/drain extension implant. After the source/drain extension implant, a spacer may be deposited in preparation for a conventional source/drain implant. Rapid thermal processing technology may be utilized to activate the implants.

An implant/rapid thermal processing technology for silicon germanium deposition may be simpler and more cost effective than epitaxial techniques from a process design perspective. In some embodiments no significant new integration schemes are necessary for implementation of the germanium implants.

By implanting germanium before the shallow source/drain extension implant, a shallower junction may be produced that has lower sheet resistivity because of the higher solid solubility of boron. In some embodiments stress is generated when the germanium concentration greatly exceeds that of boron. Referring to Figure 6, the humps indicated by the arrows labeled "strain" are indicative of a strained lattice in some embodiments.

In some embodiments, the ratio of germanium to boron ions may be approximately 4 to 1. Generally, it is advantageous to have a ratio of germanium to boron ions greater than 1 to 1, because at 1 to 1 the atoms are complementary and cancel out the lattice strain.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: